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EXAMINER	
DARE, RYAN A	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,410	PRESLER-MARSHALL, MARTIN JOSEPH CLAYTON	
	Examiner	Art Unit	
	Ryan Dare	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-6, 8-9, 11, 13-16, 18-19, 21, and 23-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Lahiri et al., US Patent 6,952,664.

3. With respect to claim 1, Lahiri et al. teach a self-tuning cache comprising:

a primary cache, in fig. 1, buffer cache 102. Throughout the specification, this buffer cache is also referred to as the "operational cache."

at least two test caches, a first one of said test caches having a cache size which is smaller than a size of said primary cache and a second one of test caches having a cache size which is greater than said size of said primary cache, in fig. 2, and described in the specification in col. 5, lines 29-56. Note that in an exemplary embodiment described therein, the size of the operational cache corresponds to one of the segment numbers, such as cache3, which corresponds to a buffer size of 1,000,000. One of the test caches, take for example cache1, has a cache size that is smaller than the

operational cache. In addition, a second one of the test caches, i.e. cache7, has a cache size that is larger than the operational cache.

a cache engine programmed to manage said primary cache and said at least two test caches, in fig. 1, cache simulation system 100.

a cache tuner coupled to said primary and test caches, said cache tuner comprising a configuration for resizing said primary cache when one of said at least two test caches demonstrates cache performance which justifies resizing said primary cache, in col. 4, lines 25-30.

4. With respect to claim 2, Lahiri et al. teach the self-tuning cache of claim 1, wherein said at least two test caches comprise a configuration for storing cache keys for cacheable objects and corresponding placeholders for said cacheable objects in lieu of storing said cacheable objects, in col. 6, lines 18-20. The data identifier mentioned by Lahiri et al. is the cache key.

5. With respect to claim 3, Lahiri et al. teach the self-tuning cache of claim 1, wherein said first one of said test caches comprises a cache size which is half that of said primary cache, in fig. 2, and described in the specification in col. 5, lines 29-56. Note that in an exemplary embodiment described therein, the size of the operational cache corresponds to one of the segment numbers, such as cache3, which corresponds to a buffer size of 1,000,000. The first one of the test caches, cache1, has a cache size that is smaller than the operational cache, precisely 500,000, which is half that of the operational cache.

6. With respect to claim 4, Lahiri et al. teach the self-tuning cache of claim 3, wherein said second one of said test caches comprises a cache size which is double that of said primary cache, in fig. 2, and described in the specification in col. 5, lines 29-56. Note that in an exemplary embodiment described therein, the size of the operational cache corresponds to one of the segment numbers, such as cache3, which corresponds to a buffer size of 1,000,000. The second one of the test caches, cache7, has a cache size that is larger than the operational cache, precisely 2,000,000 which is double that of the operational cache.

7. With respect to claim 5, Lahiri et al. teach the self-tuning cache of claim 1, further comprising a maximum limit and a minimum limit for resizing said primary cache, in fig. 2, and described in the specification in col. 5, lines 29-56. In this embodiment, the minimum limit of cache size is 250,000, and the maximum limit of cache size is 2,000,000 for the test caches. Since the size of the operational cache is adjusted to be the same size as one of the test caches, the size of the operational cache cannot be adjusted to be less than this minimum or more than this maximum limit.

8. With respect to claim 6, Lahiri et al. teach a method for self-tuning an active cache, the method comprising the steps of:

managing the active cache by inserting, retrieving and evicting cacheable objects and corresponding caching keys in the active cache and by locating cached objects selected for retrieval from the active cache by reference to corresponding ones of said caching keys, in col. 4, lines 31-47. Throughout the reference, the caching keys are referred to as "references". The simulated caches model the operational cache, which

uses the LRU replacement scheme (col. 3, lines 49-51). It can be seen in fig. 1 that the data reference is applied to buffer cache 102 (the active cache), which in turn inserts, retrieves and evicts cacheable objects according to the LRU policy.

further managing a test cache by inserting and evicting in said test cache caching keys and dummy placeholders for cacheable objects not stored in said test cache and by locating in said test cache individual ones of said caching keys corresponding to requested ones of said cacheable objects, in col. 2, lines 10-18;

measuring and comparing hit rates for each of said active cache and said test cache, in fig. 3B, step 324; and,

if said measured hit rates compare such that a change in size for the active cache is justified, resizing the active cache and said test cache, in fig. 3B, step 326, and col. 1, lines 61-64. In an embodiment described in col. 5, lines 57-62, the simulated caches are described as proportions to the operational cache. Thus, when you change the size of the operational cache, the sizes of the simulated caches are also changed in the next iteration.

9. With respect to claim 8, Lahiri et al. teach the method of claim 6, wherein said resizing step comprises:

if said test cache is larger in size than the active cache and if said test cache demonstrates a hit rate which significantly exceeds a hit rate measured for the active cache, resizing the active cache to a larger size, in col. 1, lines 61-64. In the case where the simulated cache is larger than the active cache and the hit rate is better than the operational cache, the operational cache is made to match the simulated cache.

10. With respect to claim 9, Lahiri et al. teach the method of claim 6, further comprising the step of limiting said resizing so as to not exceed a minimum and a maximum cache size for the active cache, in fig. 2, and described in the specification in col. 5, lines 29-56. In this embodiment, the minimum limit of cache size is 250,000, and the maximum limit of cache size is 2,000,000 for the test caches. Since the size of the operational cache is adjusted to be the same size as one of the test caches, the size of the operational cache cannot be adjusted to be less than this minimum or more than this maximum limit.

11. With respect to claim 11, Lahiri et al. teach a method for self-tuning an active cache, the method comprising the steps of:

receiving a request to retrieve an object, in col. 1, line 65 through col. 2, line 3;

generating a cache key for said object, in col. 2, lines 15-16;

searching the active cache for said object using said generated cache key, in col. 4, lines 31-47. With reference to fig. 1, the cache key (data reference) is applied to the buffer (active) cache 102.

further searching at least one test cache for a stored cache key which matches said generated cache key, in col. 2, lines 3-5;

returning said object from the active cache if said object is located in the active cache in said searching step, in col. 1, line 65 through col. 2, line 3;

updating hit rate statistics for each of the active cache and said at least one test cache based upon whether said objected is located in the active cache in said

searching step, and whether said generated cache key matches a stored cache key in said at least one test cache, in col. 2, lines 5-9; and,

determining whether to resize the active cache based upon said updated hit rate statistics, in col. 1, lines 61-64.

12. With respect to claim 13, Lahiri et al. teaches the method of claim 11, wherein said determining step comprises the step of:

if said at least one test cache is larger in size than the active cache and if said at least one test cache demonstrates a hit rate which significantly exceeds a hit rate measured for the active cache, resizing the active cache to a larger size, in col. 1, lines 61-64. In the case where the simulated cache is larger than the active cache and the hit rate is better than the operational cache, the operational cache is made to match the simulated cache.

13. With respect to claim 14, Lahiri et al. teaches the method of claim 11, further comprising the step of evicting stored cache keys from said at least one test cache, in col. 3, lines 49-51.

14. With respect to claim 15, Lahiri et al. teaches the method of claim 11, further comprising the step of inserting a generated cache key into said at least one test cache, in col. 3, lines 49-51.

15. With respect to claims 16, 18 and 19, Applicant claims a machine readable storage having stored thereon a computer program for performing the method of claims 6, 8 and 9, respectively, and is therefore rejected using similar logic.

16. With respect to claims 21, and 23-25, Applicant claims a machine readable storage having stored thereon a computer program for performing the method of claims 11 and 13-15, respectively, and is therefore rejected using similar logic.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

19. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

20. Claim 7, 12, 17 and 22 rejected under 35 U.S.C. 103(a) as being unpatentable over Lahiri et al., US Patent 6,952,664, as applied to claims 1-6, 8-9, 11, 13-16, 18-19, 21, and 23-25 above.

21. With respect to claim 7, Lahiri et al. teaches all limitations of the parent claim, as discussed supra, but fails to expressly disclose resizing the active cache to a smaller

size if the hit rate of the active cache does not differ significantly from the hit rate of a smaller test cache. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made, having the teachings of Lahiri et al. before him to perform this modification. Lahiri et al. teaches in col. 1, lines 16-18 that memory is wasted if a cache is too large. This fact is also acknowledged in Applicant's background of the invention, because it is desirable to find an optimal cache size, instead of having an arbitrary large cache size. Therefore, it would be obvious to the skilled artisan, in the case where the test cache is smaller in size than the active cache and if said test cache demonstrates a hit rate which does not differ significantly from a hit rate measured for the active cache (per the corrected size comparison in fig. 3b, step 324), to resize the active cache to a smaller size, as in fig. 3b, step 326.

22. With respect to claim 12, Lahiri et al. teaches all limitations of the parent claim, as discussed supra, but fails to expressly disclose resizing the active cache to a smaller size if the hit rate of the active cache does not differ significantly from the hit rate of a smaller test cache. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made, having the teachings of Lahiri et al. before him to perform this modification. Lahiri et al. teaches in col. 1, lines 16-18 that memory is wasted if a cache is too large. This fact is also acknowledged in Applicant's background of the invention, because it is desirable to find an optimal cache size, instead of having an arbitrary large cache size. Therefore, it would be obvious to the skilled artisan, in the case where the test cache is smaller in size than the active cache and if said test cache demonstrates a hit rate which does not differ significantly from a hit rate measured for

the active cache (per the corrected size comparison in fig. 3b, step 324), to resize the active cache to a smaller size, as in fig. 3b, step 326.

23. With respect to claim 17, Applicant claims a machine readable storage that performs the method of claim 7, and is therefore rejected using similar logic.

24. With respect to claim 22, Applicant claims a machine readable storage that performs the method of claim 12, and is therefore rejected using similar logic.

25. Claims 10 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lahiri et al., US Patent 6,952,664, as applied to claims 1-6, 8-9, 11, 13-16, 18-19, 21, and 23-25 above, in view of Sachedina et al., US PG Pub 2003/0204698.

26. With respect to claim 10, Lahiri et al. teaches all other limitations of the parent claim as discussed supra, but fails to expressly teach rearranging the underlying data structure based upon a change in size for the active cache. Sachedina et al. teach the method of claim 6, further comprising the step of rearranging a data structure for the active cache based upon a change in size for the active cache, in par. 26.

27. It would have been obvious to one of ordinary skill in the art, having the teachings of Lahiri et al. and Sachedina et al. before him at the time the invention was made, to modify the cache resizing method of Lahiri et al. with the hash resizing method of Sachedina et al. in order to improve performance and minimize cache misses, as taught by Sachedina et al. in par. 16.

28. With respect to claim 20, Applicant claims a machine readable storage that performs the method of claim 10, and is therefore rejected using similar logic.

Response to Arguments

29. Applicant's arguments filed 6/1/06 have been fully considered but they are not persuasive.

30. With respect to Applicant's arguments on pages 2-3 regarding claim 1, the examiner respectfully disagrees. The term cache size, as used by Applicant and Lahiri refers to the number of entries/buffers in a cache. The cache size is not the size of the database environment in which the cache simulation system exists as Applicant suggests, quoting col. 5 line 64 through col. 6, line 3 of Lahiri. Col. 3, lines 49-55, among other places in the Lahiri reference, equates cache size with the number of entries. Since one of the simulated caches has more entries/buffers that the primary cache, Lahiri does teach a test cache with a cache size greater than the primary cache.

31. With respect to Applicant's arguments on pages 3-5 regarding claims 6 and 16, the Examiner has modified the above rejections to further clarify how Lahiri teaches the limitations of claims 6 and 16. The Examiner is not relying on inherency, as it is now clear from the above rejection that Lahiri clearly discloses all limitations of claims 6 and 16.

32. With respect to Applicant's arguments on page 5 regarding claims 11 and 21, the Examiner has modified the above rejections to further clarify how Lahiri teaches the disclosed limitation.

33. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention

where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to one of ordinary skill in the art, having the teachings of Lahiri et al. and Sachedina et al. before him at the time the invention was made, to modify the cache resizing method of Lahiri et al. with the hash resizing method of Sachedina et al. in order to improve performance and minimize cache misses, as taught by Sachedina et al. in par. 16.

34. With respect to Applicant's argument that on pages 6-7, the Examiner agrees that a reference that qualifies as "prior art" only under 35 U.S.C. 102(e) cannot be considered when determining whether an invention is obvious under 35 U.S.C. 103, provided the prior art and the claimed invention were commonly owned at the time of the invention. However, this is not the case in the present application. U.S. Patent Publication 2003/0204698 (Sachedina) was published October 30, 2003. The present application, 10/759,410, was filed on Jan 16, 2004. Therefore the Sachedina reference qualifies as prior art under 35 U.S.C. 102(a) as well as 35 U.S.C. 102(e).

Conclusion

35. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan Dare whose telephone number is (571)272-4069. The examiner can normally be reached on Mon-Fri 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan A. Dare
August 18, 2006

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